REMARKS

Claims 1, 2, 4-19, 21, and 22 were pending in this application.

Claims 6-17 and 19 have been allowed.

Claims 1, 2, 4, 5, 21 and 22 have been rejected.

Claim 18 has been objected to.

No claims have been amended.

Claims 1, 2, 4-19, 21, and 22 remain pending in this application.

Reconsideration and full allowance of Claims 1, 2, 4-19, 21, and 22 are respectfully requested.

I. ALLOWABLE CLAIMS

The Applicants thank the Examiner for the indication that Claims 6-17 and 19 are in condition for allowance. These claims have not been amended and therefore remain in condition for allowance.

The Applicants also thank the Examiner for the indication that Claim 18 would be allowable if rewritten in independent form to incorporate the elements of its base claim and any intervening claims. Because the Applicants believe that the remaining claims in this application are allowable, the Applicant has not rewritten Claim 18 in independent form.

II. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1, 2 and 4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,647,485 to Nguyen et al. ("*Nguyen*") in view of U.S. Patent No. 5,001,629 to Murakami et al. ("*Murakami*"). The Office Action rejects Claims 5 and 22 under 35 U.S.C. § 103(a) as being unpatentable over *Nguyen* and *Murakami* in further view of Applicant Admitted Prior Art ("*APA*"). The Office Action rejects Claim 21 under 35 U.S.C. § 103(a) as being unpatentable over *Nguyen* and *Murakami* in further view of U.S. Patent No. 6,636,747 to Harada et al. ("*Harada*"). These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (*MPEP § 2142*).

Regarding independent Claim 1, Section 4 of the December 27, 2005, Office Action asserts that *Nguyen* describes a plurality of interface registers in register array 472 and a plurality of function units in functional units 478_{0-n}, shown in Figure 5 and described at column 32, lines 31-56. The Office Action acknowledges that *Nguyen* does not teach a plurality of register transfer units that facilitate transfers of data among interface registers. Nonetheless, the Office Action asserts that *Nguyen* describes a datapath unit that facilitates a transformation of a data item that are transferred among the interface registers, citing Figure 5 and column 32, line 50, through column 33, line 35. The Applicants respectfully submit that the Office Action mischaracterizes the teaching of *Nguyen*.

The passage in *Nguyen* cited in the Office Action as purportedly teaching a datapath unit that facilitates a transformation of a data item that are transferred among the interface registers

(identified in the Office Action as register array 472) is reproduced here for the Examiner's convenience:

> The control path portion of the IEU 104 is responsible for issuing, managing, and completing the processing of information through the IEU data path. In the preferred embodiments of the present invention the IEU control path is capable of managing the concurrent execution of multiple instructions and the IEU data path provides for multiple independent data transfers between essentially all data path elements of the IEU 104. The IEU control path operates in response to instructions received via the instruction/operand bus 124. Specifically, instruction sets are received by the EDecode unit 490. In the preferred embodiments of the present invention, the EDecode 490 receives and, decodes both instruction sets held by the IFIFO master registers 216, 224. The results of the decoding of all eight instructions is variously provided to a carry checker (CRY CHKR) unit 492, dependency checker (DEP CHKR) unit 494, register renaming unit (REG RENAME) 496, instruction issuer (ISSUER) unit 498 and retirement control unit (RETIRE CTL) 500.
>
> The carry checker unit 492 receives decoded information about the eight pending instructions from the EDecode unit 490 via control lines 502. The function of the carry checker 492 is to identify those ones of the pending instructions that either affect the carry bit of the processor status word or are dependent on the state of the carry bit. This control information is provided via control lines 504 to the instruction issuer unit 498.
>
> Decoded information identifying the registers of the register file 472 that are used by the eight pending instructions as provided directly to the register renaming unit 496 via control lines 506. This information is also provided to the dependency checker unit 494. The function of the dependency checker unit 494 is to determine which of the pending instructions reference registers as the destination for data and which instructions, if any, are dependant on any of those destination registers. Those instructions that have register dependencies are identified by control signals provided via the control lines 508 to the register rename unit 496.
>
> Finally, the EDecode unit 490 provides control information identifying the particular nature and function of each of the eight pending instructions to the instruction issuer unit 498 via control lines 510. The issuer unit 498 is responsible for determining the data path resources, particularly of the availability of particular functional units, for the execution of pending instructions. In accordance with the preferred embodiments of the architecture 100, instruction issuer unit 498 allows for the out-of-order execution of any of the eight pending instructions subject to the availability of data path resources and carry and register dependency constraints. The register rename unit 496 provides the instruction issuing unit 498 with a bit map, via control lines 512 of those instructions that are suitably

> unconstrained to allow execution. Instructions that have already been executed (done) and those with register or carry dependencies are logically removed from the bit map.

In the first paragraph, the cited passage describes the processing of instructions received by instruction execution unit (IEU) 104. The instructions are decoded by Edecode unit 490 and the results distributed to carry checker unit 492, dependency checker unit 494, register renaming unit 496, instruction issuer unit 498 and retirement control unit 500. The second paragraph states that instructions that affect, or are dependent on, the carry bit are identified to the carry checker unit 492. The third paragraph describes that the registers of register file 472 that are used by an instruction are identified to register renaming unit 496 and dependency checker unit 494. The fourth paragraph teaches that instruction issuer unit 498 is responsible for the execution of instructions using functional units 478_{0-n}.

The Office Action does not indicate where in these four paragraphs *Nguyen* describes a datapath unit that facilitates a transformation of a data item that are transferred among interface registers. The Office Action identifies the register array 472 as teaching the recited plurality of interface registers, however, the only mention in the cited passage of the register array 472 is in the third paragraph. There, the registers affected by an instruction are identified to the register renaming unit 496 and the dependency checker unit 494. However, no transformation of the data items transferred among the registers of register array 472 is taught in the cited passage, other than that performed by functional units 478_{0-n} in the performance of the instruction. The functional units 478_{0-n} are identified in the Office Action as teaching the plurality of function units recited in the claim, rather than the recited "at least one datapath unit."

Thus, the cited passage describes the processing of instructions received in EDecode unit 490, rather than teaching a datapath unit, operably coupled to a plurality of register transfer units, that facilitates a transformation of at least one data item of data that is transferred among interface registers, as recited in independent Claim 1. For these reasons, the Office Action does not establish a *prima facie* case of obviousness against Claim 1 (and its dependent claims). Accordingly, the Applicants respectfully request withdrawal of the § 103 rejections and full allowance of Claims 1, 2, 4, 5, 21 and 22.

IV. CONCLUSION

For the reasons given above, the Applicants respectfully request reconsideration and full allowance of all pending claims and that this application be passed to issue.

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SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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William A. Munck
Registration No. 39,308

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *wmunck@davismunck.com*